Mystery Circuits 2

Download the Logisim file called “mystery circuits 2” which contains several related circuits. Explore these circuits to determine and understand their functionality and composition.

Mystery Circuits 1

The first two circuits in this file are related, implementing the same functions. The first one is viewed as a “black box” and the second one shows the circuit structure inside the box. Start with the “mystery 1 box” circuit. You can see that it has 8 inputs (X7 through X0) and 4 outputs (Z2 through Z0 and R). This circuit has been designed with the assumption that **no more than one** of the X inputs will be asserted (i.e. set to 1) at a time; we’ll relax that assumption in the next circuit.

Toggle the inputs one at a time (ensuring that only one input is asserted at a time) and observe the outputs. **Describe in words the functionality of mystery circuit 1**.

Mystery circuit 1 outputs represent bits and result in 1 according to the input number. For instance, X0 is on, the output is Z0, Z1, Z2, are all off because X0 = bit 0. If X4 is enabled, then Z2 is set it 1 because X4= 4 bits

Unassert (i.e. set to zero) all X inputs and then toggle the X0 input. This action should reveal the purpose of the R output. **Describe the function of the R output here**.

R indicates were the inputs are valid (on) and not valid (off)

Before you look inside the box, write a truth table below that describes the function of mystery circuit 1. Although there are 8 inputs, there are only 9 possible input combinations to consider, so the truth table is not very large. Using your truth table derive the logic functions for each of the outputs.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | Which one? | Z2 | Z1 | Z0 | R |
| 1 | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **7** | T | T | T | T |
| 0 | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **6** | T | T | F | T |
| 0 | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **5** | T | F | T | T |
| 0 | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **4** | T | F | F | T |
| 0 | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **3** | F | T | T | T |
| 0 | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **2** | F | T | F | T |
| 0 | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | F | F | T | T |
| 0 | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | F | F | F | T |
| 0 | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **None** | F | F | F | F |

**Z2 = X7 + X6 + X5 + X4**

**Z1 = X7 +X6+X3+X2**

**Z0 = X7 +X5 +X3 + X1**

**R = X7+X6+X5+X4+X3+X2+X1+X0**

Now look “inside the box” and verify that your logic functions are correct.

Mystery circuits 2

Mystery circuit 2 is similar to mystery circuit 1, with three differences. First it only has 4 inputs rather than 8; this is because the logic functions are a little more complex and 4 inputs keeps the manual design process feasible. The second difference is more important: we’ve relaxed the assumption that only one input is asserted at a time. Finally, the R output is **active low**.

First, assert one input at a time and determine whether the circuit behaves the same as mystery 1 in these cases**. Note any differences here:**

Enabling the inputs results in the signals turning from 0 to 1, for all inputs R turns to 0

Next, assert multiple inputs and examine the outputs. **Describe your findings here:**

The output corresponds to the lowest bit order of input, no matter how many inputs there are. When X3, X2, X1 are on, the output displays Z0 being true which is the same as X1 just itself. When X3 and X2 are on, the result is Z1, which is the same as just X2 being on.

The truth table for this circuit is interesting; **fill it in below.** **Derive one of the output functions and verify it with the circuit implementation in “mystery 2 insides.”**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| X3 | X2 | X1 | X0 | Which one? | Z1 | Z0 | R |
| x | **x** | **x** | **1** | **0** | 0 | 0 | 0 |
| x | **x** | **1** | **0** | **1** | 0 | 1 | 0 |
| x | **1** | **0** | **0** | **2** | 1 | 0 | 0 |
| 1 | **0** | **0** | **0** | **3** | 1 | 1 | 0 |
| 0 | **0** | **0** | **0** | **none** | T | T | T |

**Z1 = X3 +X2**

**Z0 = X3 +X1**

**R = none**

**Write words to describe the function of this circuit**.

To make Z0 to be true, X0 has to be false and X1 has to be true or both X0 and X2 have to be false

Composition of functions

In order to facilitate the composition of larger circuits from smaller ones, an enable has been added and is shown in the “mystery 2 with enable” circuit. Look at this circuit and admire it.

Next look at the composition of two “mystery 2” circuits to create a larger one. Examine the R output from the upper box; it’s the enable for the lower one. **Do you see now why the R output was changed to be active low?**

R output was changed to be active low because it signifies if the circuit is on or off. R is true when the circuit has no high bit inputs and when the circuit is off with lower bit inputs.

**Describe what’s going on with the two MUXes on the right.**

The output is similar to mystery 2 as the outputs Z2, Z1, and Z0 come from the lowest bit order of input. However, the main difference is that the lower half of the bit inputs are controlled by the enable button

Using library components

The last circuit in this file shows how to use the priority encoder from the library**. Explore this circuit to determine**

* **Whether the enables are active high or active low**
* **Whether the R output is active high or active low**
* **Which input has the highest priority and which has the lowest.**

Notice the address outputs (what we were calling Z in the earlier circuits). These outputs are now multiple bits treated as one value. **Why is one MUX sufficient here when we needed more than one on mystery circuit 2?**

On mystery circuit 2, each of the three outputs had 1 bit while the MUX of the priority encoder circuit has 1 output with 3 bits. The three outputs on mystery circuit 2 represented a 3 bit output.

Observe how a splitter is used to add the 4th bit (the MSB) to the 3 output bits of the MUX. You’ll need to use a splitter later in this class.

Highest priority would be 15 and lowest priority would be zero.